REMARKS

Claims 1, 2 and 5-14 are pending in the present application. Claims 1 and 2 have been amended. Claims 5-14 have been presented herewith. Claims 3 and 4 have been canceled. Applicant respectfully reserves the right to file a divisional application including claims 3 and 4.

Priority Under 35 U.S.C. 119

A Claim of Priority has been filed concurrently herewith along with Japanese Priority Application No. 2003-370863. **The Examiner is respectfully requested to acknowledge receipt of the certified copy of the priority document, and to confirm that the Claim for Priority under 35 U.S.C. 119 is complete**.

Information Disclosure Statement

Enclosed are copies of an Information Disclosure Statement and Form PTO-1449 filed along with the present application on January 22, 2004. Also enclosed is a copy of a dated, stamped postcard receipt provided as evidence that the Information Disclosure Statement and PTO-1449 Form were received by the U.S. Patent Office along with the corresponding references. **The Examiner is respectfully requested to acknowledge receipt of the Information Disclosure Statement, and to confirm that the references cited therein have been considered and will be cited of record**.

Claim Objections

Claims 1 and 2 have been objected to in view of the informalities as listed on page 2 of the current Office Action dated May 17, 2005. Claims 1 and 2 have been corrected as requested by the Examiner. The Examiner is therefore respectfully requested to withdraw the objection to the claims.

Claim Rejections-35 U.S.C. 103

Claims 1 and 2 have been rejected under 35 U.S.C. 103(a) as being unpatentable over the Chiu et al. reference (U.S. Patent No. 4,514,897) in view of the Fujii et al. reference (U.S. Patent No. 5,017,979). This rejection is respectfully traversed for the following reasons.

The method of manufacturing a nonvolatile semiconductor storage device of claim 1 includes in combination "...a second step of patterning the first polysilicon layer and the first insulating film into the shape of a band"; and "a third step of thermally oxidizing the patterned band-shaped first polysilicon layer, thereby to form a second insulating film which is thicker at side surfaces of the first polysilicon layer than at the front surface thereof...". Applicant respectfully submits that method of manufacturing a nonvolatile semiconductor storage device of claim 1 would not have been obvious in view of the prior art as relied upon by the Examiner.

The Examiner has alleged that the Chiu et al. reference discloses "to form a second insulating film (24) which is thicker at side surfaces of the first polysilicon layer

(13) than at the front surface thereof", as illustrated in Fig. 2 and 7 for example. However, contrary to the Examiner's assertion, the Chiu et al. reference does not specifically describe that silicon dioxide layer 24 is thicker at side surfaces of floating gate 13 than at a front surface of floating gate 13.

As described in column 3, lines 15-16 of the Chiu et al. reference with respect to Fig. 2, "The control gate 14 is isolated from the floating gate by a thermal oxide layer 24". As further described in column 6, lines 60-66 of the Chiu et al. reference with respect to Fig. 5d, silicon dioxide layer 24 is grown on the first level polysilicon, producing a coating on all exposed surfaces of the poly including tops and sides. Silicon dioxide layer 24 is grown at about 1100°C in O_2 for about 55 minutes and in N_2 for 30 minutes, "producing about 1200 Å thickness and consuming part of the polysilicon".

Accordingly, the above noted portions of the Chiu et al. reference specifically describe that silicon dioxide layer 24 is coated on all exposed surfaces of the underlying poly as having a thickness of "about 1200 Å". Silicon dioxide layer 24 is not disclosed or even remotely suggested as being specifically formed so as to be thicker on side surfaces of floating gate 13 than on a front surface thereof, as alleged by the Examiner.

The Examiner has apparently solely relied upon the illustrations of the device structure in Figs. 2 and 7 of the Chiu et al. reference to assert that silicon dioxide layer 24 is thicker on side surfaces of floating gate 13. However, the Chiu et al. reference does not specify that Figs. 2 and 7 are drawn to scale. The Chiu et al. reference also

fails to specifically describe that silicon dioxide layer 24 is particularly grown in such a manner so as to be formed thicker on side surfaces of floating gate 13 than on a front surface of floating gate 13. As noted above, silicon dioxide layer 24 is described as merely grown as "a coating on all exposed surfaces of the poly... producing about 1200 Å thickness". In absence of any specific description in the Chiu et al. reference, and/or reasoning as offered by the Examiner that would establish why silicon dioxide layer 24 would be formed thicker on side surfaces of floating gate 13 in view of the specific processing parameters set forth therein, it must be considered that any perceived difference in thickness of silicon dioxide layer 24 in Figs. 2 and 7 of the Chiu et al. reference is merely incidental.

Applicant therefore respectfully submits that the Chiu et al. reference as primarily relied upon by the Examiner does not meet the features regarding the second insulating film thickness of claim 1. The secondarily relied upon Fujii et al. reference does not overcome the above noted deficiency of the Chiu et al. reference. Applicant therefore respectfully submits that the method of manufacturing a non-volatile semiconductor storage device of claim 1 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection is improper for at least these reasons.

The method of manufacturing a non-volatile semiconductor storage device of claim 2 includes in combination "...a second step of implanting nitrogen ions into a front surface of the first polysilicon layer"; and "a third step of thermally oxidizing the first

polysilicon layer implanted with the nitrogen ions, thereby to form a second insulating film which is thicker at side surfaces of the first polysilicon layer than at the front surface thereof...".

Applicant respectfully submits that the prior art as relied upon by the Exmainer, particularly the Chiu et al. reference, does not specifically describe a second insulating film formed on a first polysilicon layer whereby the second insulating film is thicker at sides surfaces of the first polysilicon layer than at a front surface thereof. Applicant therefore respectfully submits that the method of manufacturing a non-volatile semiconductor storage device of claim 2 would not have been obvious in view of the prior art as relied upon by the Examiner taken singularly or together, and that this rejection is improper for at least these reasons.

Claims 5-14

Applicant respectfully submits that claims 5 and 6 as dependent upon claim 1, and claims 7 and 8 as dependent upon claim 2, distinguish over and would not have been obvious in view of the prior art as relied upon by the Examiner, by virtue of dependency upon claims 1 and 2 respectively for the reasons as set forth above.

Moreover, claims 5 and 7 feature that "the nitrogen ions are implanted into the first polysilicon layer so as to be located only in the front surface of the first polysilicon layer". The Examiner has apparently interpreted barrier layer 43 in Fig. 14A of the Fujii et al. reference as the implanted nitrogen ions of the claims. However, as described in

column 10, lines 22-27 of the Fujii et al. reference, "Oxygen and nitrogen ions **are locally implanted** into the polysilicon film 42 so as to cover a region above the tunnel insulating film 41. The resultant structure is then subjected to a heat treatment so that a barrier layer 43 for impurity diffusion is formed in the polysilicon film 42" (our emphasis added).

Accordingly, as may be readily understood in view of the above noted description and as illustrated in Fig. 14A of the Fujii et al. reference, barrier layer 43 is not implanted into polysilicon film 42 so as to be located only in the front surface of polysilicon film 42, as would be necessary to meet the features of claims 5 and 7. Particularly, barrier layer 43 is locally implanted into the polysilicon film 42 appreciably below the surface of polysilicon film 42. Barrier layer 43 is not located at the surface of polysilicon film 42. Applicant therefore respectfully submits that claims 5 and 7 distinguish over and would not have been obvious in view of the prior art as relied upon by the Examiner for at least these additional reasons.

Regarding claim 6 and 8, as described on page 7, lines 17-22 of the present application with respect to Fig. 3A, nitrogen ions are implanted into the front surface of the polysilicon layer 14A **so as to stay in only the front surface**. The implantation conditions of nitrogen ions to achieve this are featured in claims 6 and 8. The Fujii et al. reference clearly does not disclose or make obvious the implantation conditions as featured in claims 6 and 8. Applicant therefore respectfully submits that claims 6 and 8 distinguish over and would not have been obvious in view of the prior art as relied upon

by the Examiner for at least these additional reasons.

The method of manufacturing a semiconductor device of claim 9 includes in combination "...implanting nitrogen ions into a front surface of the first polysilicon layer"; and "thermally oxidizing the band-shaped segment to simultaneously grow a second insulating film on side surfaces and the front surface of the first polysilicon layer, wherein the second insulating film is thicker on the side surfaces of the first polysilicon layer than on the front surface of the polysilicon layer implanted with nitrogen ions...".

As emphasized previously, the prior art as relied upon by the Examiner does not specifically disclose a second insulating film formed on a first polysilicon layer, wherein the second insulating film is formed thicker on side surfaces of the first polysilicon layer than on a front surface thereof. Applicant therefore respectfully submits that the method of manufacturing a semiconductor device of claims 9-14 distinguish over and would not have been obvious in view of the prior art as relied upon by the Examiner for at least the above reasons.

Conclusion

The Examiner is respectfully requested to reconsider and withdraw the corresponding rejection, and to pass the claims of the present application to issue, for at least the above reasons.

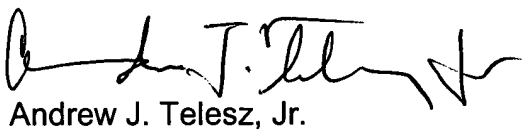
In the event that there are any outstanding matters remaining in the present application, please contact Andrew J. Telesz, Jr. (Reg. No. 33,581) at (571) 283-0720

in the Washington, D.C. area, to discuss these matters.

If necessary, the Commissioner is hereby authorized in this, concurrent, and future replies, to charge payment for any additional fees that may be required, or credit any overpayment, to Deposit Account No. 50-0238.

Respectfully submitted,

VOLENTINE FRANCOS & WHITT, P.L.L.C.



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Enclosures: Copies of Information Disclosure Statement and Form PTO-1449 dated January 22, 2004
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